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10/809,925	03/25/2004	Hiroshi Yamazaki	1324.70190	6761

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,925	YAMAZAKI, HIROSHI	
	Examiner	Art Unit	
	Sarvesh J. Nadkarni	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 March 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 7/15/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed March 25, 2004, Application Number: 10/809,925 (hereinafter referred to as "application"). The application was published on November 18, 2004, Publication Number: US 2004/0227715 A1. Page and line number references made in this action relate to the originally filed application, not the publication. Receipt is acknowledged of the information disclosure statement, form PTO-892, filed on July 15, 2004.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. FIG. 19 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 through 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The terms "IC", "ICs", and Ics" are used in the above mentioned claims and are not properly defined in the specification, and therefore, render these claims indefinite. Appropriate correction is required. Strictly for purposes of examination these terms will collectively be understood as a short form of integrated circuit(s).

6. Furthermore, claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "input capacitance of the first clock signal" is not clearly defined in the specification, and therefore, renders this claim indefinite. Appropriate correction is required. Strictly for purposes of examination, this phrase will collectively be understood as any capacitance value of a signal line.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 7, 9, 10, and 11 are rejected under 35 U.S.C. 102(b) based upon a public use or sale of the invention in view of Go, United States Patent Number 6,320,566 B1, Date of Patent: November 20, 2001 (hereinafter referred to as "Go '566").

9. With regard to claim 7, Go '566 discloses **a liquid crystal display device** (see column 1, lines 10-11) **comprising: a liquid crystal display panel;** (see column 1, lines 34-47) **a plurality of data driver ICs for driving data lines of the liquid crystal display panel;** (see column 3, lines 33-38) **a first clock signal line** (see column 4, line 11, "first clock signal" furthermore see FIG. 10 element labeled "FD1" and column 6 lines 21 "first clock signal FD1) **for transmitting a first clock signal to the plurality of data driver Ics** (see column 4, lines 22-25) **a second clock signal line** (see column 4, line 11, "second clock signal" furthermore see FIG. 10 element labeled "FD2" and column 6 lines 22 "first clock signal FD2) **which is equipped in parallel with the first clock signal line** (see FIGs. 10 and 12, clock signal lines FD1 and FD2 are drawn in parallel) **and transmits a second clock signal which is in reverse relation with the first clock signal;** (see column 4, lines 10-13, describing the signals having a180 degree phase difference, furthermore, see FIG 11, showing the phase difference) **and a timing controller for outputting the first and second clock signals to the first and second**

clock signal lines respectively;(see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **wherein the data driver ICs input the first and second clock signals, and can selectively latch data signals with the first or second clock signal.** (see column 4, lines 20-28 describing latching data signals and gates to selectively latch to even or odd lines).

10. With regard to claim 9, Go '566 discloses **a data driver IC** (see column 1, line 52 "data driver IC 11") **for a liquid crystal display device,** (see column 1, lines 10-11) **characterized in that the data driver IC inputs a first clock signal** (see column 4, line 11, "first clock signal") **and a second clock signal** (see column 4, line 11, "second clock signal") **in reverse relation with the first clock signal,** (see column 4, lines 11-13, describing the phase of the signals being 180 degrees apart; furthermore see column 4, lines 20-27 describing the second clock having a reverse polarity relative to the first clock signal) **latches data signals of odd-number dots with the first clock signal** (see column 4, lines 20-24) **and latch data signals of even-number dots with the second clock signal** (see column 4, lines 24-28).

11. With regard to claim 10, it is similarly analyzed as claim 9 above. "Selectively latching" is much broader in claim 10 as opposed to claim 9 because the latching may occur with either the first or second clock signals. Therefore claim 10 is rejected on the same grounds and analysis as claim 9.

12. With regard to claim 11, Go '566 discloses **a timing controller** (see column 4 line 10, "clock signal generator") **for a liquid crystal display device,** (see column 4 lines 1-2) **characterized in that data signals of odd-number dots and data signals of even-**

number dots (see column 4, lines 20-24) **are output every horizontal line** (see FIG. 6A and 6B described in column 2, lines 46-48 in conjunction with FIG. 10 further described at column 6, lines 20-25) **while displacing the phase between the data signals of the odd-number dots and even-number dots by 180 degrees.** (see column 6, lines 20-25).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Go, United States Patent Number 6,320,566 B1, Date of Patent: November 20, 2001 (hereinafter referred to as "Go '566") and further in view of Misawa et al., United States Patent Number: 5,616, 936, Date of Patent: April 1, 1997 (hereinafter referred to as "Misawa '936").

15. With regard to claim 1, Go '566 discloses **a liquid crystal display device** (see column 1, lines 10-11) **comprising: a liquid crystal display panel;** (see column 1, lines 34-47) **a plurality of data driver ICs for driving data lines of the liquid crystal display panel;** (see column 3, lines 33-38) **a first clock signal line** (see column 4, line 11, "first clock signal" furthermore see FIG. 10 element labeled "FD1" and column 6 lines 21 "first clock signal FD1) **for transmitting a first clock signal to the plurality of data driver Ics** (see column 4, lines 22-25) **a second clock signal line** (see column 4, line 11, "second clock signal" furthermore see FIG. 10 element labeled "FD2" and

column 6 lines 22 "first clock signal FD2) **which is equipped in parallel with the first clock signal line** (see FIGs. 10 and 12, clock signal lines FD1 and FD2 are drawn in parallel) **and transmits a second clock signal which is in reverse relation with the first clock signal;** (see column 4, lines 10-13, describing the signals having a180 degree phase difference, furthermore, see FIG 11, showing the phase difference) **and a timing controller for outputting the first and second clock signals to the first and second clock signal lines respectively;**(see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100")

16. However, Go '566 fails to teach **a load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first clock signal line.**

17. However, Misawa '936 teaches **a load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first clock signal line**. (see column 20, lines 15-25, the "source line driving circuit" performs this function).

18. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the source line driving circuit as disclosed in Misawa '936 into the liquid crystal display device of Go '566 because, as disclosed in column 12 lines 17-46 of Misawa '936, equalizing the capacitance reduces the added noise and improves picture quality, both of which are consistently progressive goals within the art

19. With regard to claim 5 as dependent on claim 1, Go '566 discloses **a data signal line for odd-number dots** (see column 4, lines 20-24, "odd data lines") **for transmitting data signals of odd-number dots** (pixel electrodes 26 are attached to the odd data lines) **and a data signal line for even-number dots** (see column 4, lines 20-24, "even data lines") **for transmitting data signals of even-number dots** (pixel electrodes 26 are attached to the odd data lines) **are equipped, and the timing controller outputs the data signals of the odd-number dots and the data signals of the even-number dots every horizontal line** (see FIG. 6A and 6B described in column 2, lines 46-48 in conjunction with FIG. 10 further described at column 6, lines 20-25) **while displacing the phase between the data signals of the odd-number and even-number dots by 180 degrees,** (see column 6, lines10-14 in conjunction with lines 20-28) **and the data driver ICs input the first and second clock signals** (see column 6, lines 19-25)**, latch the data signals of the odd-number dots with the first clock signal and latch the data signals of the even-number dots with the second clock signal** (see column 6, lines 20-28).

20. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 and Misawa '936 as applied to claim 1 above, and further in view of Toyoshima et al., United States Patent, Patent Number US 6,795,049 B2, Date of Patent: September 21, 2004 (hereinafter referred to as "Toyoshima '049").

21. With regard to claim 2, Go '566 in view of Misawa '936 teaches **the liquid crystal display device according to claim 1.** However, Go '566 in view of Misawa '936 fail to teach the **load means is constructed by equipping dummy terminals to the data driver ICs, and connecting the second clock signal line to the dummy terminals.**

22. However, Toyoshima '049 discloses **the load means is constructed by equipping dummy terminals** (column 5, lines 31-33, describing dummy element) **to the data driver ICs** (see FIG 4, further described in column 7, lines 43-59), **and connecting the second clock signal line to the dummy terminals** (see FIG 4. further described in column 7, lines 43-59; the second clock line is connected to the dummy lines).

23. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the dummy terminal configuration of Toyoshima '049 into the display device of Go '566 in view of Misawa '936 because Toyoshima '049 provides for stable operation of the display device and a reduced area of elements outside of the display region (see column 1, lines 55-60).

24. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 in view of Misawa '936 as applied to claim1 above, and further in view of Drake et al., United States Patent, Patent Number 6,339,413 B1, Date of Patent: January 15, 2002 (hereinafter referred to as Drake '413).

25. With regard to claim 3 Go '566 in view of Misawa '936 discloses **the liquid crystal display device according to claim 1,** However, Go '566 in view of Misawa '936 fails to teach **the load means is constructed by containing a capacitor in a terminating circuit.**

26. In the same field of endeavor, Drake '413 clearly teaches **the load means is constructed by containing a capacitor in a terminating circuit** (see Figure 6 element 108 used to reduce or eliminate noise and is connected to ground, furthermore, see column 10, lines 37-40).

27. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate display device of Go '566 in view of Misawa '936 into the drive circuit of Drake '413 because the design of Drake '413 reduces noise in the circuit (see column 10, lines 37-40).

28. With regard to claim 4 and as dependent on claim 3, Misawa '936 discloses having another capacitance value having the **same capacitance value as the input capacitance of the first clock signal of the data driver ICs.** Namely, Misawa '936 clearly discloses equalizing the capacitance of the two clock signal lines with the signal bus, and therefore equating the two clock lines. Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to have combined the terminal capacitor of Drake '413 into the equalizing capacitance design of Misawa because such a design would further reduce the noise in the circuit (see column 10, lines 37-40 of Drake '413).

29. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Go '566" in view of Misawa '936 and further in view of Ogata et al., Japanese Patent Number JP 407329337A. Hereinafter referred to as "Ogata".

30. With regard to claim 6, Go '566 discloses **A timing controller** (see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **for a liquid crystal display device** (see column 1, lines 10-11). However, neither Go '566, nor Misawa '936 teach **output pins for data signals are arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.**

31. Ogata discloses **data signal of an odd-number dot of each bit of each color** (see abstract "data signal having odd bits") **of each bit** (see abstract "of one line") **and the data signal of an even-number dot** (see abstract "data signal having even bits") **of the same bit** (see abstract "of one line") **are adjacent to one another** (see demonstrative FIG 1 illustrating odd lines 1, 3...n-1 adjacent to even lines 2, 4... n-1).

32. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the display device of Go '566 and Misawa '936 into the data signal line arrangement of Ogata because as disclosed in the purpose portion of the abstract of Ogata, the arrangement "reduces the capacity of power source" and "prevents the decrease of image quality level."

33. Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Go '566" and further in view of Ogata et al., Japanese Patent Number JP 407329337A. Hereinafter referred to as "Ogata".

34. With regard to claim 12, Go '566 discloses **A timing controller** (see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **for a liquid crystal display device** (see column 1, lines 10-11). However, Go '566 fails to discloses **output pins for data signals are arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.**

35. Ogata discloses **output pins** (see demonstrative FIG 1 illustrating odd lines 1, 3...n-1 adjacent to even lines 2, 4... n-1) **for data signal of an odd-number dot of each bit of each color** (see abstract "data signal having odd bits") **of each bit** (see abstract "of

one line") **and the data signal of an even-number dot** (see abstract "data signal having even bits") **of the same bit** (see abstract "of one line") **are adjacent to one another** (see demonstrative FIG 1 illustrating odd lines 1, 3...n-1 adjacent to even lines 2, 4... n-1).

36. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the display device of Go '566 into the data signal line arrangement of Ogata because as disclosed in Ogata, the arrangement "reduces the capacity of power source" and "prevents the decrease of image quality level."

37. With regard to claim 8, it is rejected on the same basis and rationale as claim 12 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarvesh J. Nadkarni whose telephone number is 571-270-1541. The examiner can normally be reached on 8:00-5:00 M-Th EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-273-1550. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJN

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